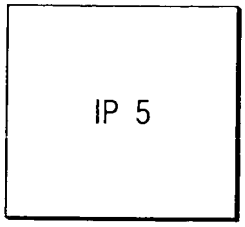


FIG. 1

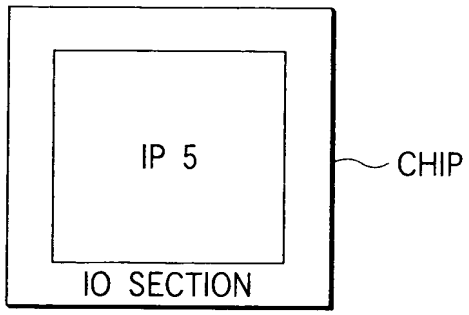


FIG. 3

FIG. 2

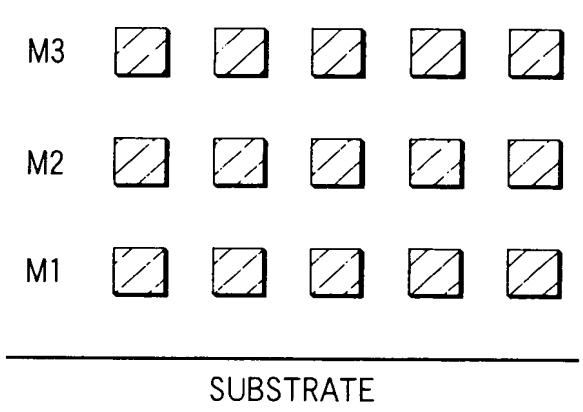
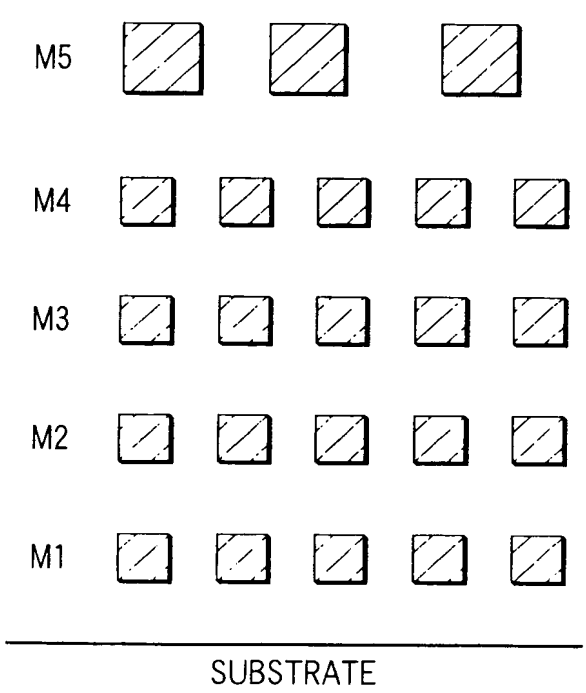


FIG. 4



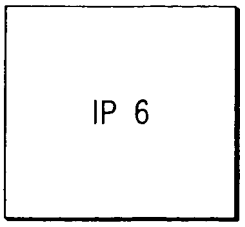


FIG. 5

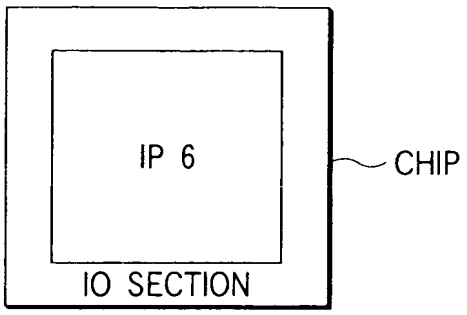


FIG. 7

FIG. 6

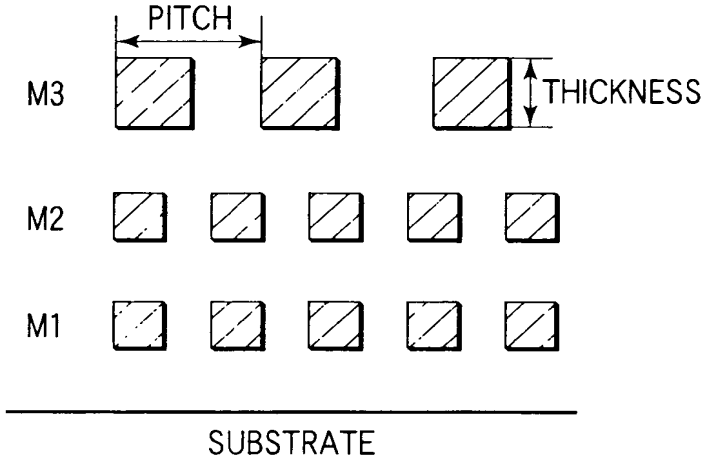
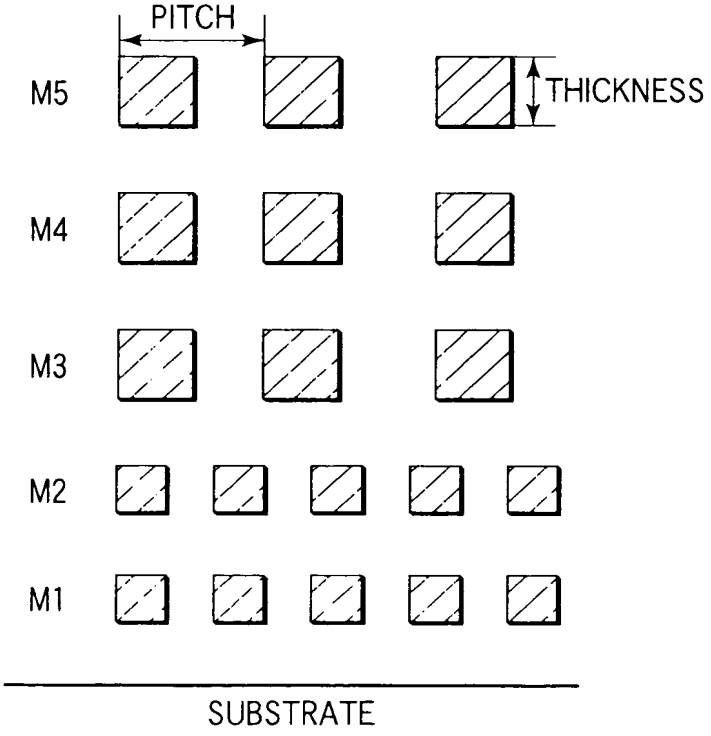


FIG. 8



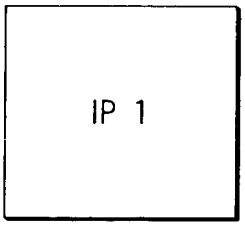


FIG. 9

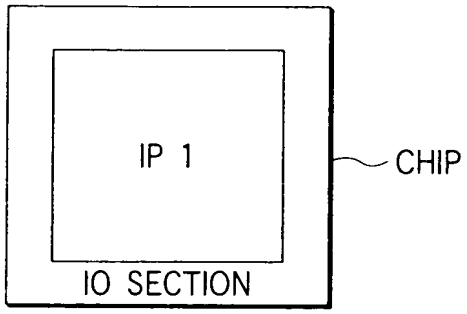


FIG. 11

FIG. 10

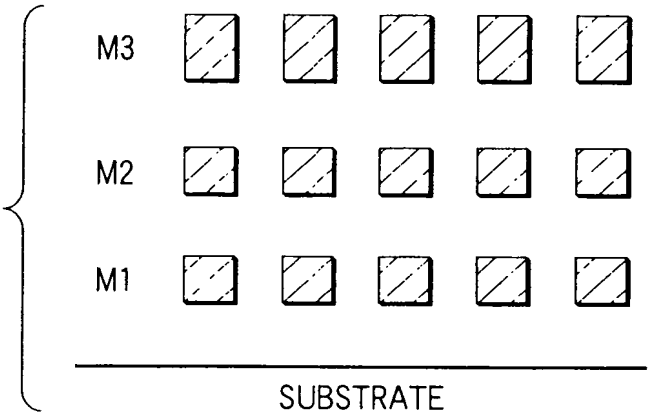
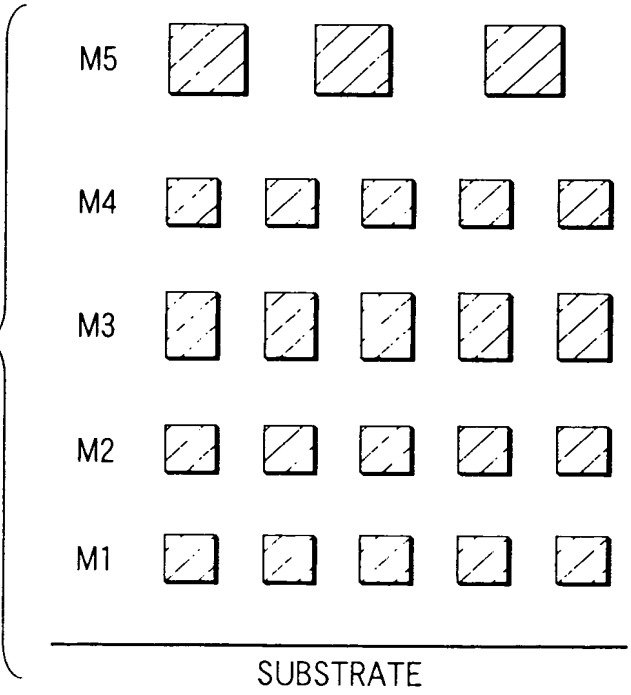


FIG. 12



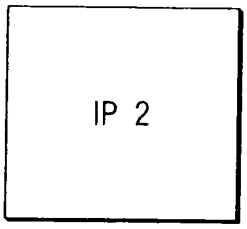


FIG. 13

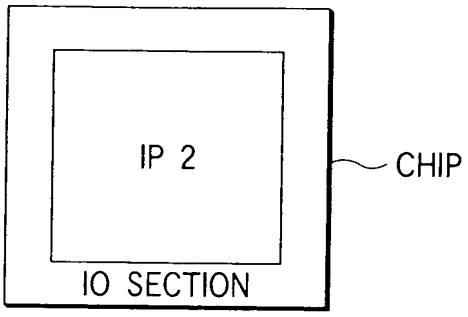


FIG. 15

FIG. 14

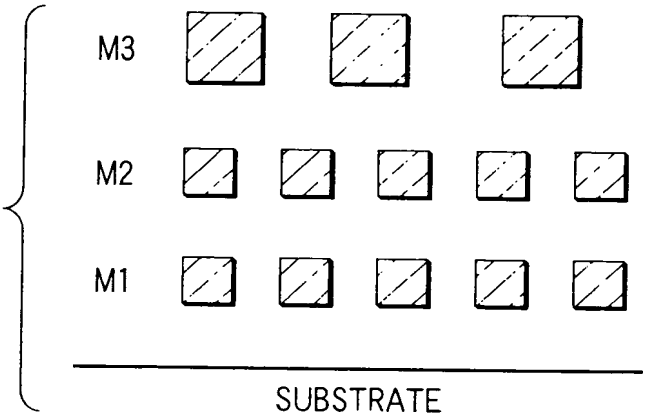
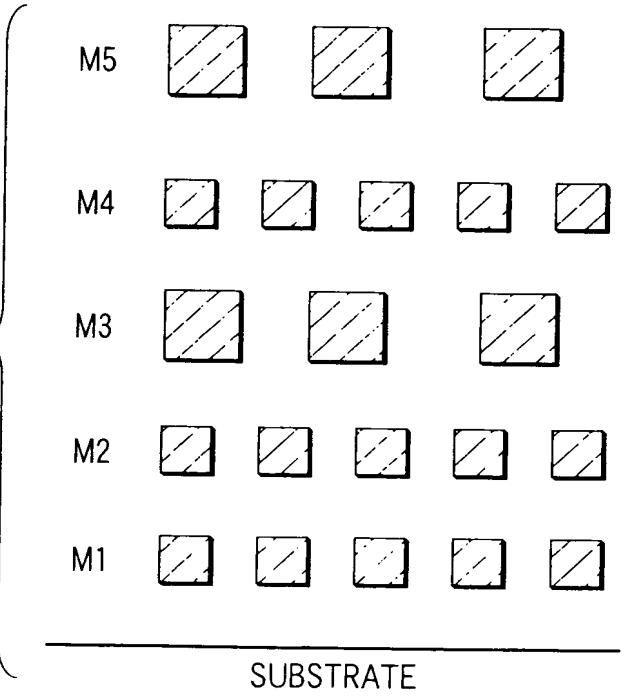


FIG. 16



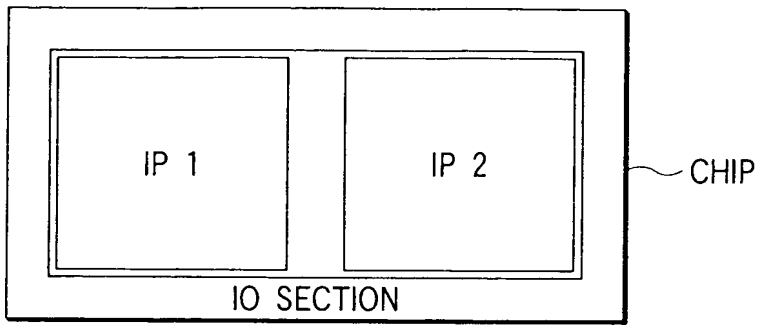


FIG. 17

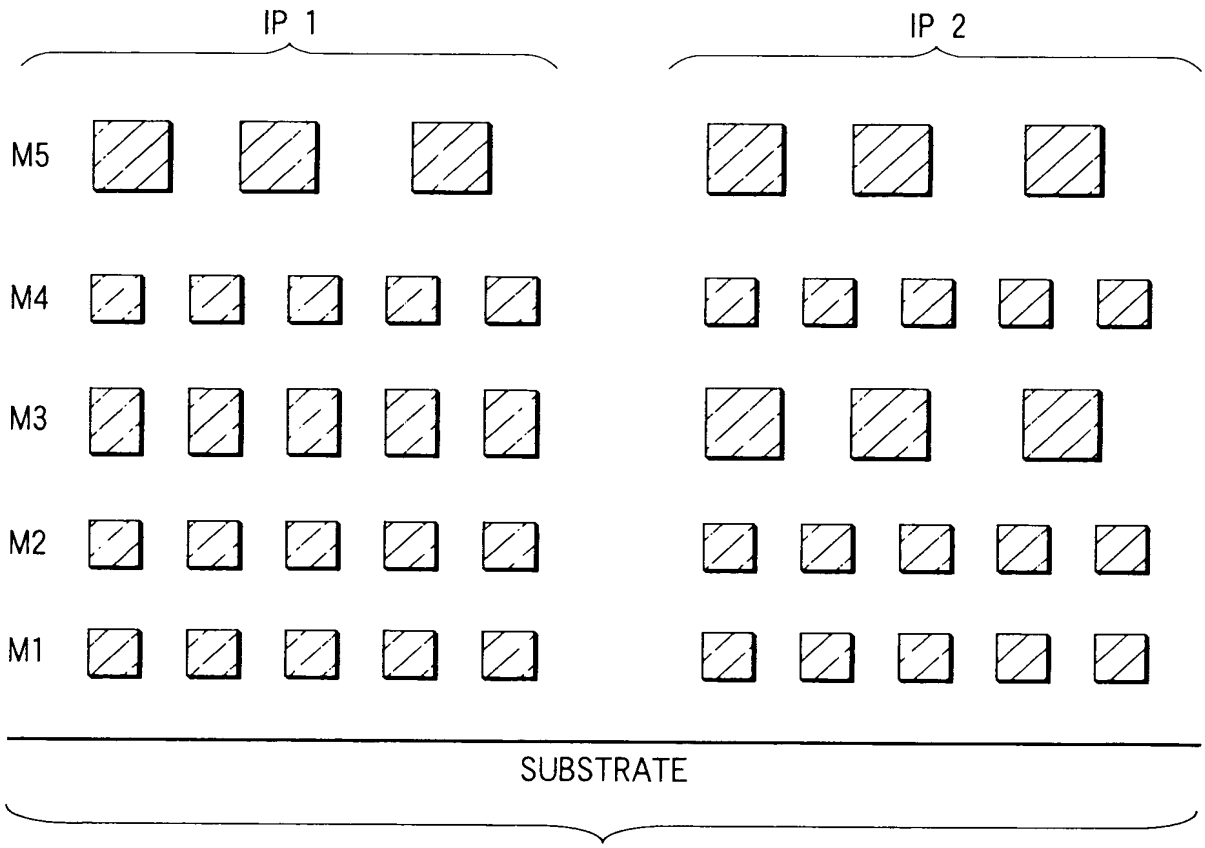


FIG. 18

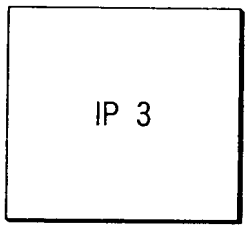


FIG. 19

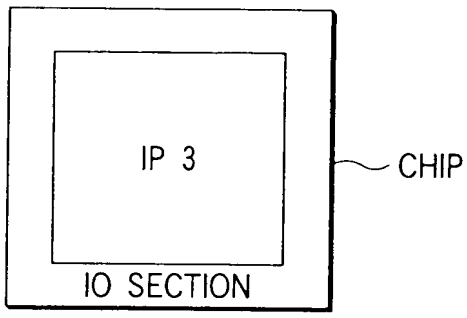


FIG. 21

FIG. 20

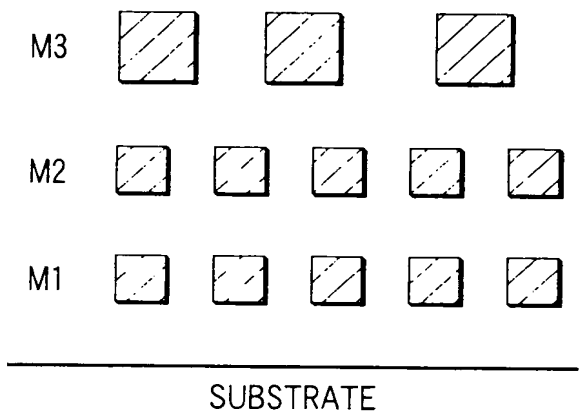
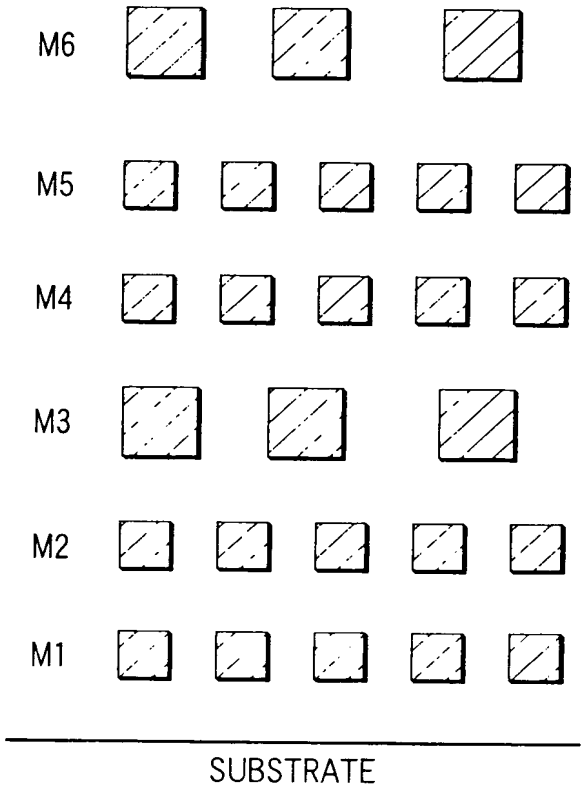


FIG. 22



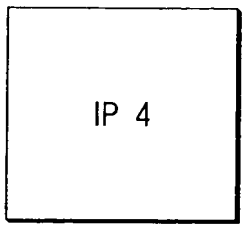


FIG. 23

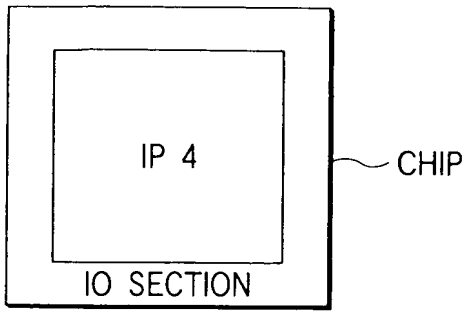


FIG. 25

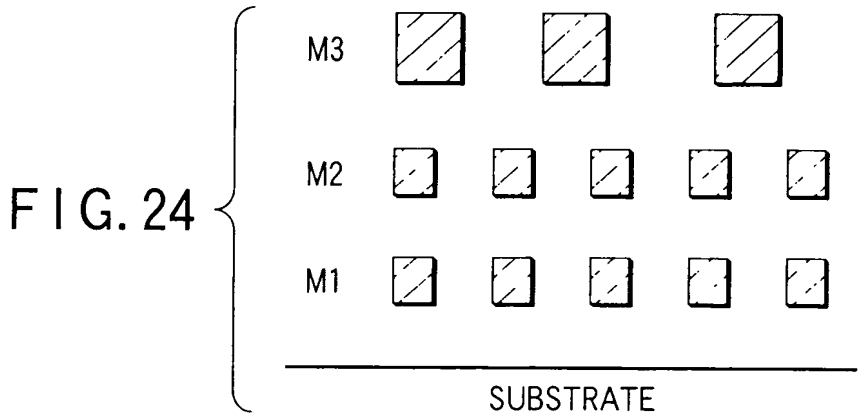


FIG. 24

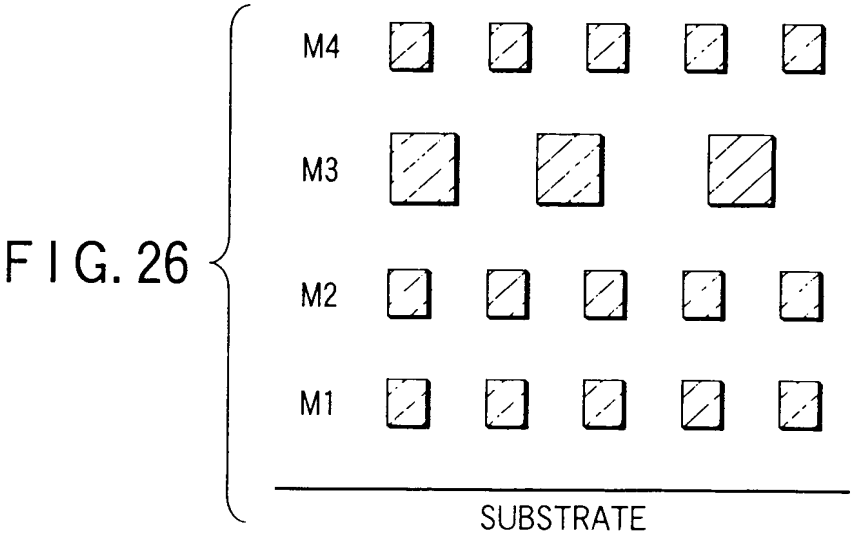


FIG. 26

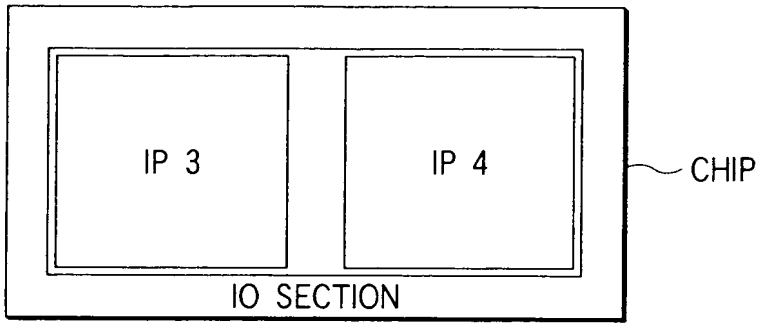


FIG. 27

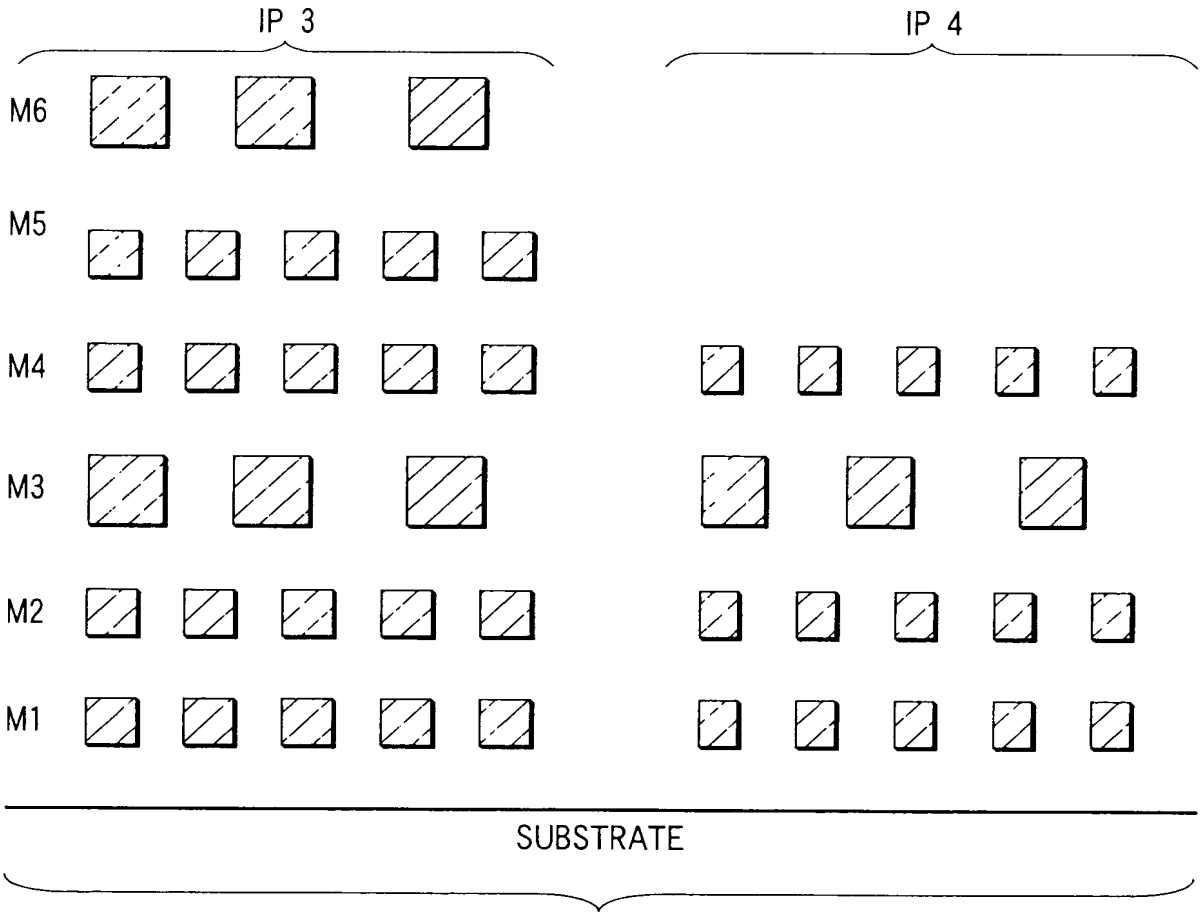


FIG. 28

	WIRING LAYER	REFERENCE EXAMPLE		PRESENT INVENTION	PURPOSE OF USING
	Mn	TK	TK TK TK	TK TK	CHIP POWER SOURCE LINE
	⋮				
	Mm+2	TN	TK TK TK	TN TK	SIGNAL LINE
	Mm+1	TN	TN TK TK	TN TN	SIGNAL LINE
IP CORE	Mm	TN	TN TN TK	TK TK	CORE POWER SOURCE LINE/ SIGNAL LINE
	⋮				
	M2	TN	TN TN TN	TN TN	SIGNAL LINE
	M1	TN	TN TN TN	TN TN	SIGNAL LINE

TK : THICK
TN : THIN

FIG. 29

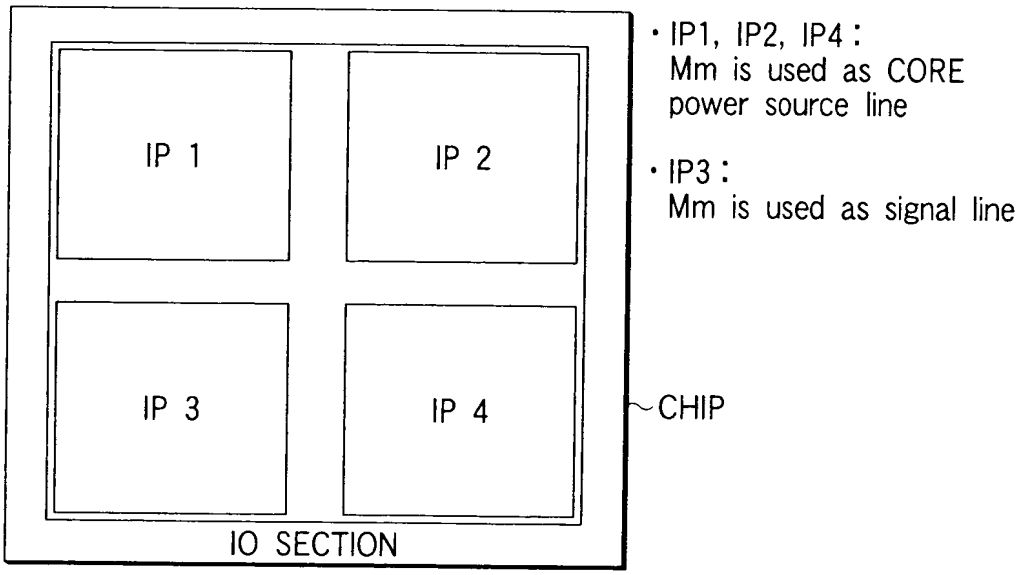


FIG. 30